24A sourcing current and sinking current Dual channel

1. Characteristics

- Dual-channel independent-grid driving
- 4A peak sourcing current and sinking current
- VDD power supply with wide ranges as high as 24V
- Independent enabling input
- With two channels, it can be applied to large current driving in a parallel way
- Optional reverse input and non-reverse input
- VDD under-voltage protection
- Compatible to TTL and CMOS input level
- Low propagation delay
- 1ns typical delay matching between two channels
- Output low level during input floating
- Working temperature ranges of -40℃ to 125℃

2.Application

- AC/DC and DC/DC converter
- Server and rectifier for communication equipment
- EV/HEV inverter and DC/DC convertor
- PV voltage rise and inverter
- UPS
- Motor control
- Applied to emerging broad-band gap power element driver

3. Description

The SL27523/4/5 are dual-channel 4A high-speed low-side gate drivers that efficiently and safely drive MOSFETs and IGBTs. Features such as low propagation delay and mismatch, and a compact SOP-8 package allow MOSFETs to switch at several hundreds of kHz. The chip is applicable to synchronous rectification driving of servers and communication power supply. In this condition, the dead time of the synchronous tube MOSFET leads to direct influence on efficiency of the converter. The driver can increase the output drive current by paralleling two channels. Input pin threshold voltages are based on TTL levels and are compatible with inputs from -5V to 20V.

The wide scope VDD supply voltage of 4.5V to 20V can effectively drive MOSFET or GaN power device.The integrated UVLO protective function can ensure the output low level in abnormal conditions. The -5V to 24V independent input pin voltage ranges can ensure stable working in condition of over-shoot caused by stray inductance. The voltage threshold value of the input pin is compatible to the TTL level input

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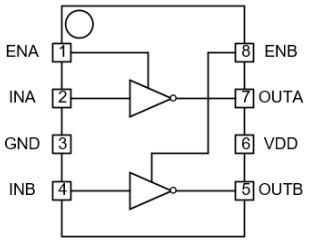
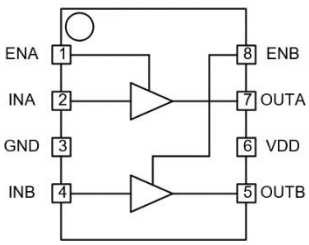
Distribution of pins

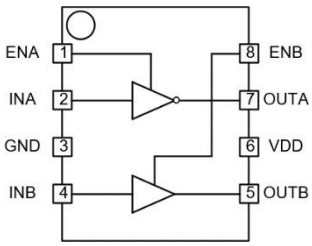
Dual-channel reverse input



dual-channel non-reverse input



One-channel reverse input and one-channel non-reverse input



Contents

4. Configuration and functions of pins

pin	Name	I/O	Description
1	ENA	I	A Channel enabling input
2	INA	I	A Channel input
3	GND	G	Ground
4	INB	I	B Channel input
5	OUTB	O	B Channel output
6	VDD	P	Supply voltage
7	OUTA	O	A Channel output
8	ENB	I	B Channel enabling input

Truth-value table

The voltage of VDD is higher than the threshold voltage of UVLO OUTx (x = A or B) is independently controlled by INx and ENx

SL27523 / 4 / 5				SL27523		SL27524		SL27525	
ENA	ENB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
High or floating	High or floating	Low	Low	Height	Height	Low	Low	Height	Low
High or floating	High or floating	Low	Height	Height	Low	Low	Height	Height	Height
High or floating	High or floating	Height	Low	Low	Height	Height	Low	Low	Low
High or floating	High or floating	Height	Height	Low	Low	Height	Height	Low	Height
Low	Low	Any level	Any level	Low	Low	Low	Low	Low	Low
Any level	Any level	floating	floating	Low	Low	Low	Low	Low	Low

5. Technical indexes

5.1 Absolute Max. rated value

Within the ranges of indoor temperature (unless otherwise specified) (1)

		MIN	MAX	Unit
V_{DD}	Supply voltage (relative to ground)	-0.3	24	V
OUTA,OUTB	Gate drive output voltage	-0.3	V_{DD}+0.3	V
INA,INB	Signal input voltage	-5	24	V
T_J	Junction temperature	-40	150	°C
T_{STG}	storage temperature	-65	150	°C

(1) If the operation exceeds the ranges listed in the "absolute maximum rated value", it may lead to permanent damages to the device. Long-term exposure to the absolute maximum rated value conditions may lead to influences on reliability of the device.

5.2 Anti-static level

		Value	Unit
$V_{(ESD)}$	Human body model(HBM)， ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	voltage live device model (CDM)，JEDEC specification JESD22-C101(2)	+/-500	

(1) As specified in JEDEC document JEP155, the standard ESD control process is allowed for safe manufacturing for 500V HBM.
(2) As specified in JEDEC document JEP155, the standard ESD control process is allowed for safe manufacturing for 250V CDM.

5.3 Working conditions

		MIN	MAX	Unit
V_{DD}	Supply voltage	4.5	20	V
$V_{INx,}$ ENx	signal input voltage	0	20	V
T_A	environment temperature	-40	125	°C

5.4 Thermal resistance information

		Value	Unit
$R_{\theta JA}$	junction temperature – environment	128	°C/W
$R_{\theta JA}$	junction temperature –PCB	68.5	°C/W

5.5 Electrical specifications

Unless otherwise specified, V_{DD} = 12 V, TA = –40°C to 125°C

In the environment of 25℃, in the designated pin, the positive-going current is input, and the inversed current is output.

Parameters	Testing conditions	MIN	Typical	MAX	Unit
Bias current					
I_{DDoff} Starting current	VDD=3V, OUTA=OUTB=0V		70		μA
I_{DDq} Quiescent current	INA=INB=0V		180		μA
Undervoltage protection(SL27524)					
V_{ON} under voltage locking threshold value VOFF	Rise threshold value		3.8	4.2	V
	Drop threshold value	3.2	3.5		
Undervoltage protection (**SL27523/5**)					
V_{ON} under voltage locking threshold value VOFF	Rise threshold value		3.8	4.25	V
	Drop threshold value	3.2	3.5		
Inverting input(INA, INB of S L 27523 and INA of S L27525)					
V_{INH} input rise threshold value			1.8	2.4	V
V_{INL} input drop threshold value		0.8	1.1		V
V_{INHYS} input hysteresis			0.8		V
V_{INHYS} negative voltage input		-5			V
non-inverting input(INA, INB of S L 27524 and INB of S L27525)					
V_{INH} input rise threshold value			2.0	2.4	V
V_{INL} input drop threshold value		0.8	1.2		V
V_{INHYS} input hysteresis			0.8		V
V_{INNS} input hysteresis		-5			V
Enabling input(ENA,ENB)					
VENH Enable Input Rising Threshold			1.8	2.2	V
V_{ENL} Enable Input Falling Threshold		0.8	1.1		V
V_{INHYS} Enable input hysteresis			0.7		V
OUTPUT (OUTA, OUTB)					
I_O Sourcing and sinking current peak	CLOAD =0.22uF, With external current limiting resistor, 1kHz switching frequency		4		A
V_{OH} output high level	IOUTH = -10mA		VDD-0.05	VDD-0.12	V
V_{OL} output low level	IOUTL = 10mA		0.0057	0.012	V
R_{OH} output quiescent pull-up resistance			5	12	Ω
R_{OL} output pull-down resistance			0.57	1.2	Ω
Time series					
TDff drop dela TDff rise dela	Cload = 1.8nF		16 16		ns
Tf drop time Tf rise time	Cload = 1.8nF		6 6		ns
T_{dm} delay mismatch	INA=INB, ENA=ENB=VDD SL27523 SL27524		1		ns

6. Typical Characteristics

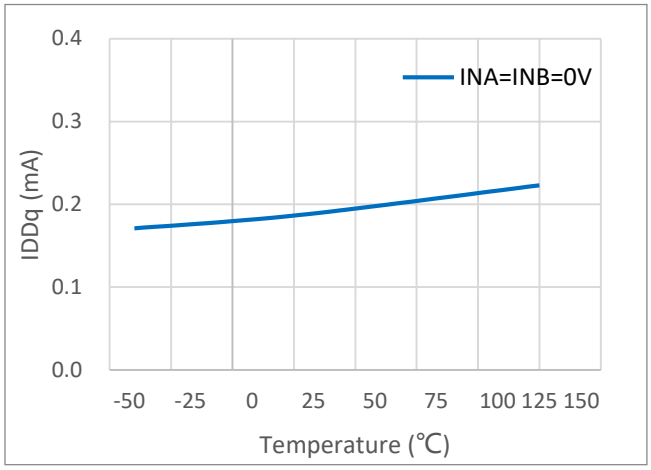


Figure 1. Quiescent current IDDq vs temperature

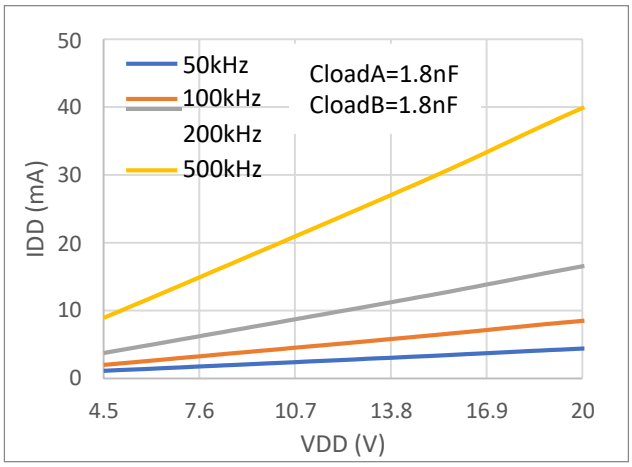


Figure 2. Working current IDDq vs VDD

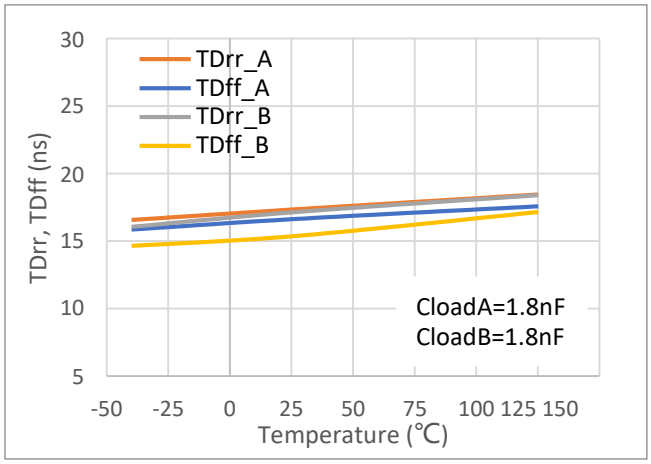


Figure 3. Propagation delay vs temperature

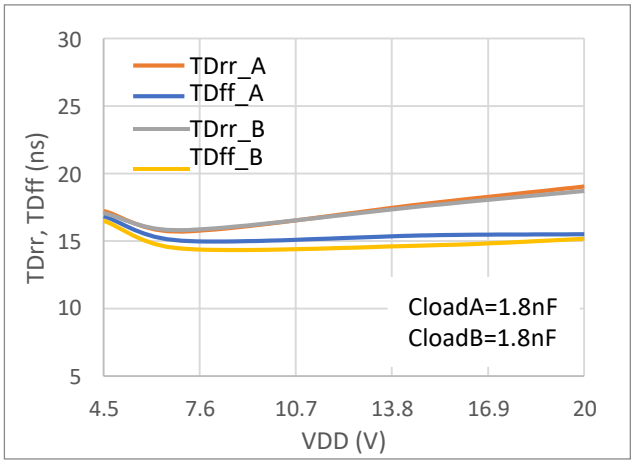


Figure 4. Propagation delay vs VDD

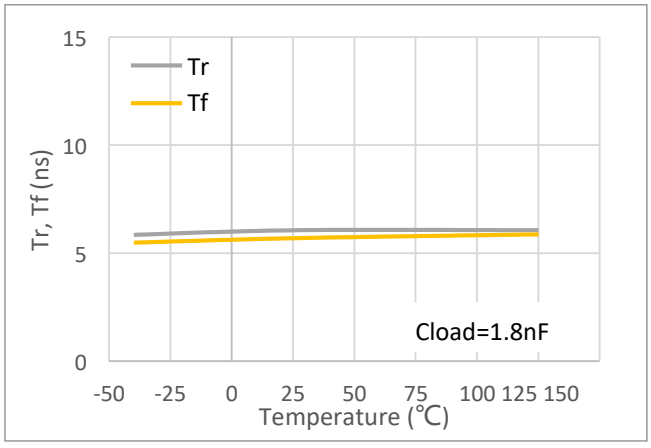


Figure 5. Rise time and drop time vs temperature

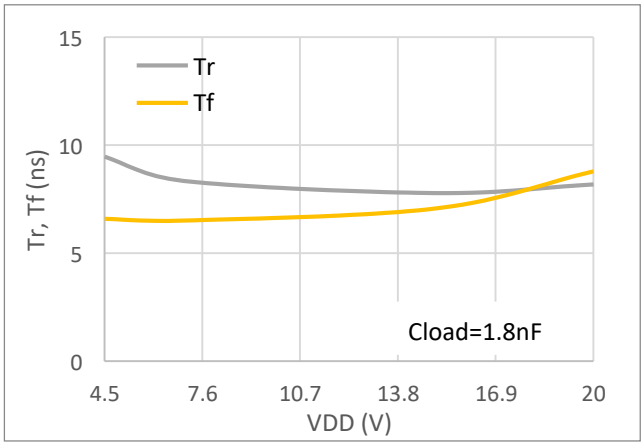


Figure 6. Rise time and drop time vs VDD

7. Detailed description

The SL27523/4/5 drivers provide dual-channel high-speed low-side gate drive. The SL27523/4 can reduce output signal mismatch when paralleling two channels to drive high power or parallel power switches.

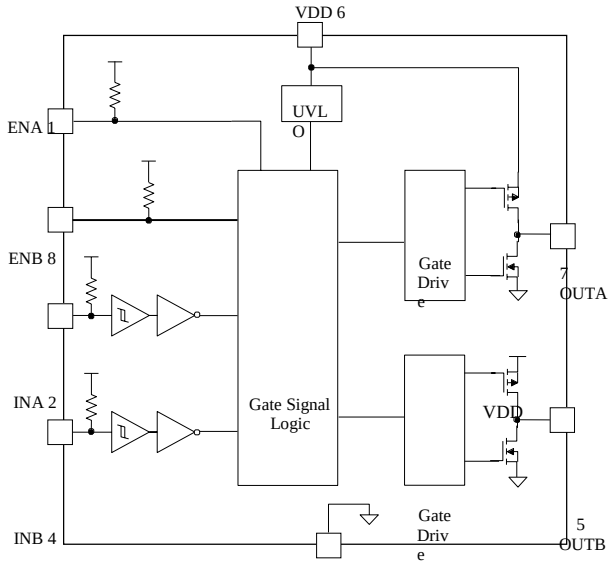


Figure 7. Functional block diagram of SL27523

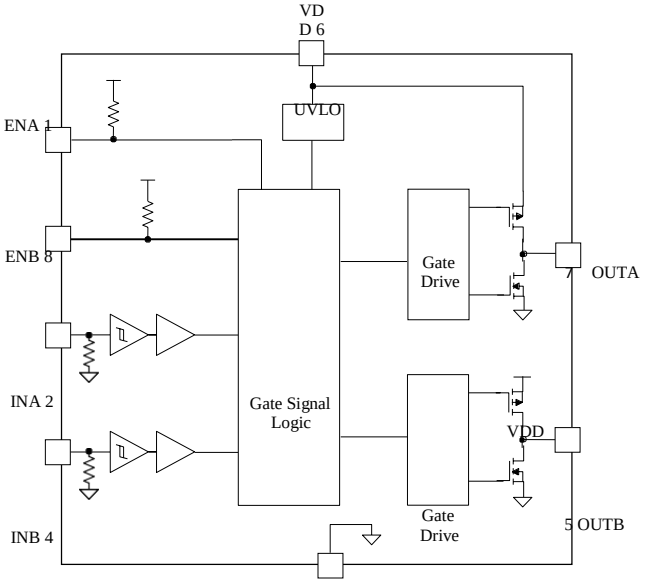


Figure 8. Functional block diagram of SL27524

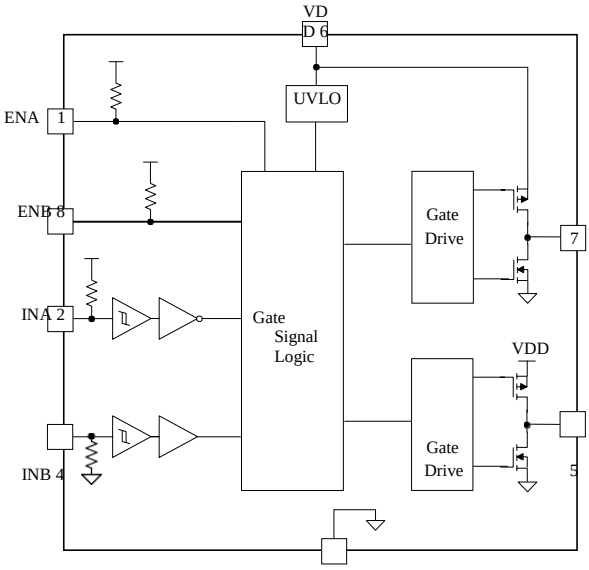


Figure 9 Functional block diagram of SL27525

7.1 Input signal INA and INB

INA and INB are grid driving input. All the reverse input pins (INA and INB of SL27523 and INA of SL27525) are pull-up input, and all the non-reverse input pins (INA and INB of SL27524 and INB of SL27525) are pull-down input. If input is kept floating, the output will be pulled to the ground. The input is the TTL and CMOS compatible logic level, with the maximum input tolerance of 24V.

7.2 Enabling signals ENA and ENB

ENA and ENB are enabling controlling signals. If the controlling signals are compatible to TTL and CMOS logic level, the maximum input tolerance is 24V When ENx is pulled low, OUTx output is low. When ENx is pulled high or floating, OUTx follows the input of Inx (INA and INB of SL27524),or OUTx is the reverse direction of Inx (INA and INB of SL27525). Enabling pin is a weak pull-up pin.

7.3 OUTA and OUTB

OUTA and OUTB are push-pull outputs, composed by a pair of complexed pull-up P model and N model MOSFET and a pull-down MOSFET. Each output of SL27523/4/5 can provide 4A sourcing current pulse and sinking current pulse. The output voltage swing in a rail-to-rail way from VDD and GND. The diode of MOSFET will also provide voltage clamping access to restrain the output voltage to exceed or lower than the ranges. In many conditions, the external Schottky diode clamping is not necessary.

7.4 VDD and undervoltage protection

The maximum rated input voltage of SL27523/4/5 is 24V, which can meet the requirements on grid driving of Si MOSFET, IGBT and SiC MOSFET. SL27511 can meet the grid driving requirements of Si MOSFET, IGBT, and SiC MOSFET. SL27511 can meet the grid driving requirements of Si MOSFET、IGBT, and SiC MOSFET.

8. Application and realization

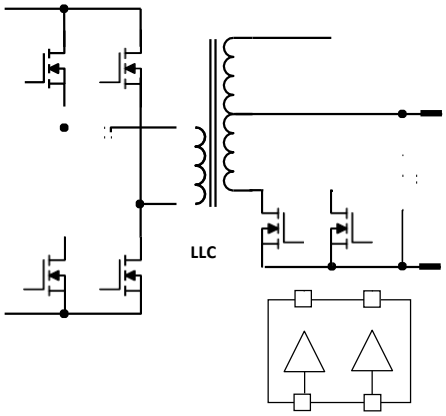


Figure 10. Driving by two channels separately (SL27523/4/5)

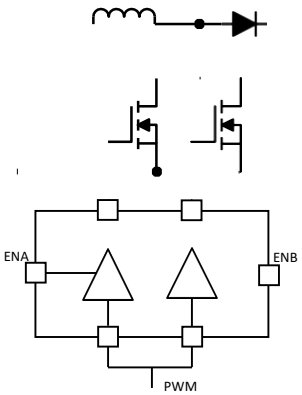


Figure 11. Two outputs drive two parallel switching devices with the minimum mismatching (SL27523/4/5)

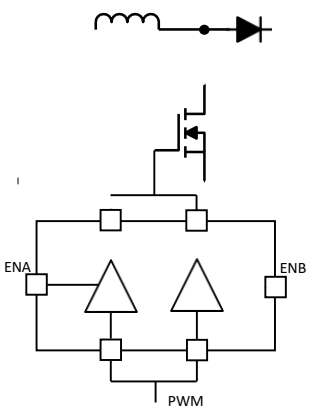


Figure 12. Two outputs drive one large power switching device in a parallel way with the minimum mismatching (SL27523/4)

9. PCB arrangement

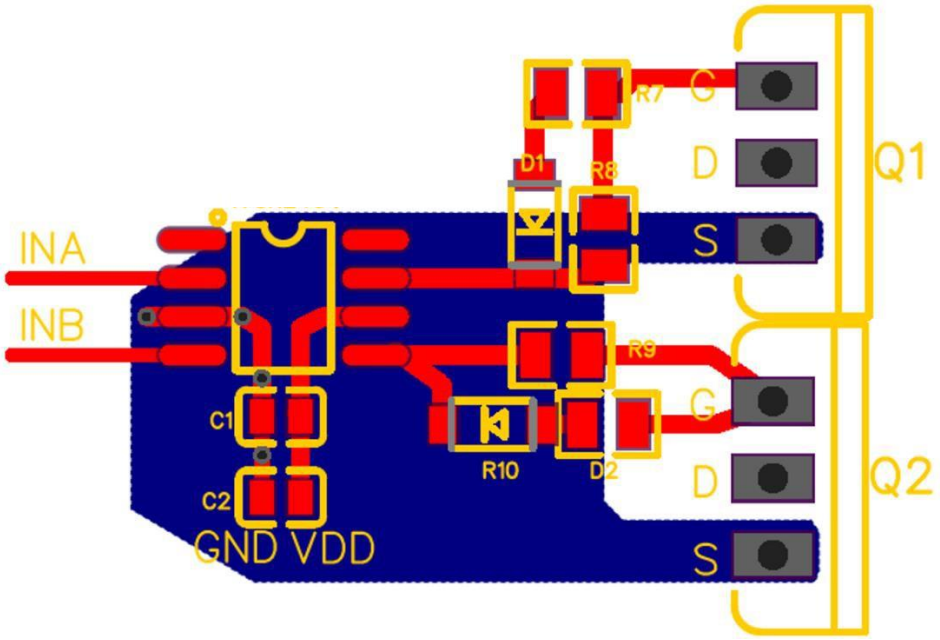
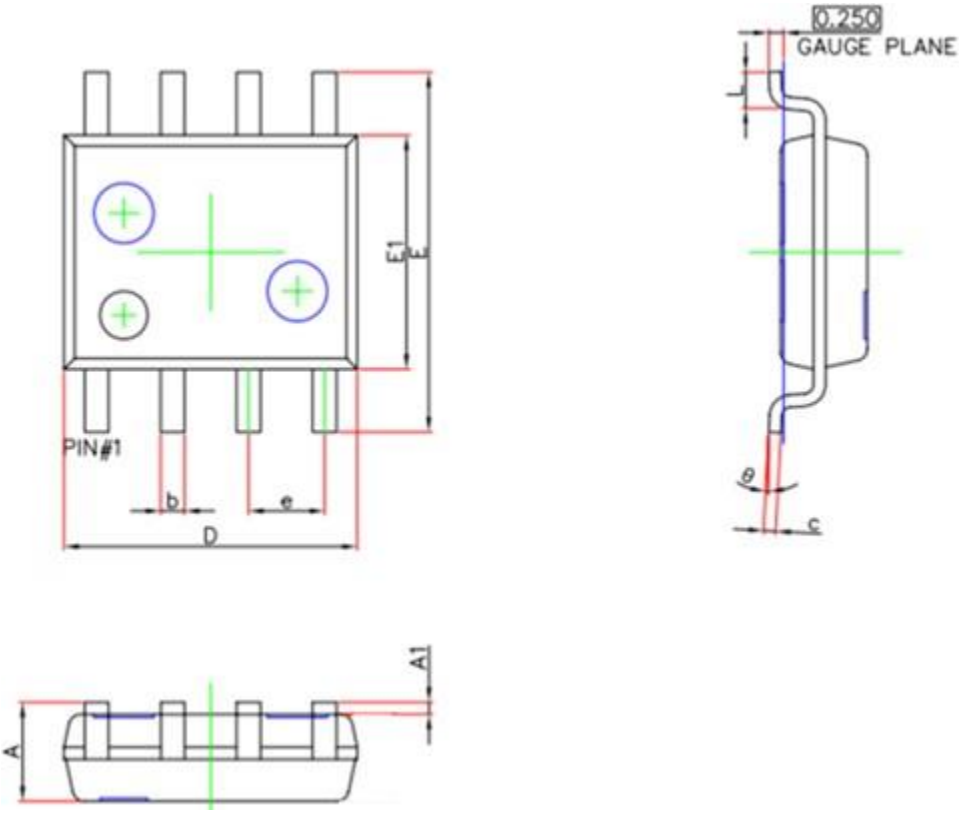


Figure 13. Case for arrangement of SL27523/4/5

10. Package information

SOP-8 package dimension



Symbol	Dimension (mm)		Dimension (inch)	
	min	max	min	max
A	1.350	1.750	0.053	0.069
A1	0.110	0.250	0.004	0.010
b	0.310	0.510	0.012	0.020
c	0.130	0.250	0.005	0.010
D	4.810	5.000	0.189	0.197
E	5.800	6.190	0.228	0.244
E1	3.810	3.980	0.150	0.157
e	1.270		0.050	
L	0.410	1.270	0.016	0.050
θ	0.000	8.000	0.000	0.315