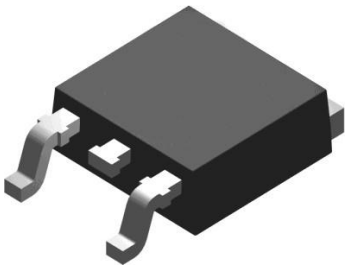
1.Function Description

SL42744D is a 3-pin TO package one-chip integrated voltage regulator, with the suggested maximum driving current of 400mA and chip package of TO252-3. The chip is applied to driving of micro-processor systems or automobile applications of several conditions; in addition, it has functions such as overloading protection, short circuit protection and over-temperature protection.

If the input voltage V1 is within the ranges of $(VQ+V_{dr}) < V1 < 42V$, it is regulated to VQ, and the voltage difference V_{dr} changes between 0.3V and 0.5V according to the size of the driving current.

2. Characteristics

- Rated output voltage 5V
- Typical output current 400mA
- Low voltage difference, with the typical value of 0.3V
- Short circuit protection
- Over-temperature protection
- Input voltage as high as 42V
- Working temperature ranges Top＝- 40～125℃
- RoHS



3. Module block diagram and pin configuration

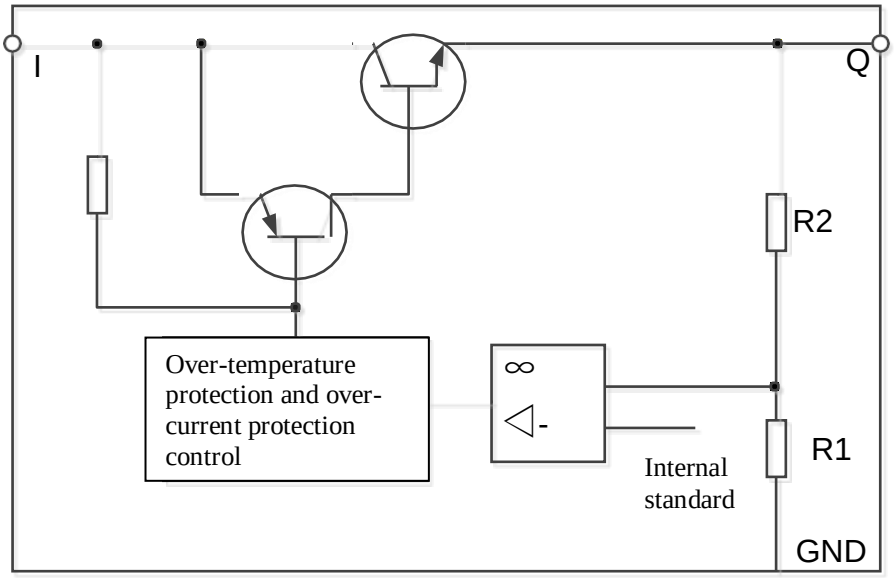


Figure 3-1SL42744D Fixed output voltage module block diagram

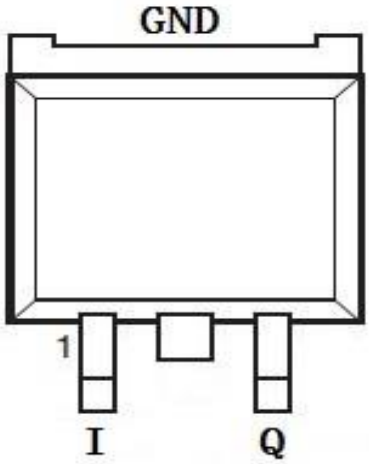


Figure 3-2 Pin configuration (top view)

Table 3.1- Pin definition and functions

No. of pin	Symbol	Function
1	I	**Input**
2	GND	**Ground:** Connect to the cooling fin in the device
3	Q	**Output** Connect a capacitor of CQ≥10uF and ESR≤10Ω at 10KHz to the ground.

4. Maximum rated value

Table 4.1 Absolute Maximum Ratings

Top=-40℃ to 150℃. All the voltage values are relative to ground unless otherwise specified.

Parameters	Symbols	Limiting value		Units	Remark
		Min	Max		
Input and output voltage difference	VI-VQ	-0.3	37	V	
Input Voltage	VI	-0.3	42	V	
Output voltage	VQ		12	V	
ESD withstanding voltage					
HBM	Voltage	-2	2	KV	1)
CDM	Voltage	-500	500	V	2)
Temperature	Tj	-40	150	℃	Junction temperature
	Tstg	-40	150	℃	Storage temperature
Thermal resistance	R_{thJA}	37	90	K/W	Without PCB

1) The ESD withstanding voltage human body model is designed according to JESD22-A114.

2) The ESD withstanding voltage charging/discharging equipment model is designed according to JESD22-C101.

Remarks: The limiting voltage listed above may lead to permanent injury to the chip, and long-term exposure in the maximum rated value may lead to influences on reliability of the device

5. Appliance property

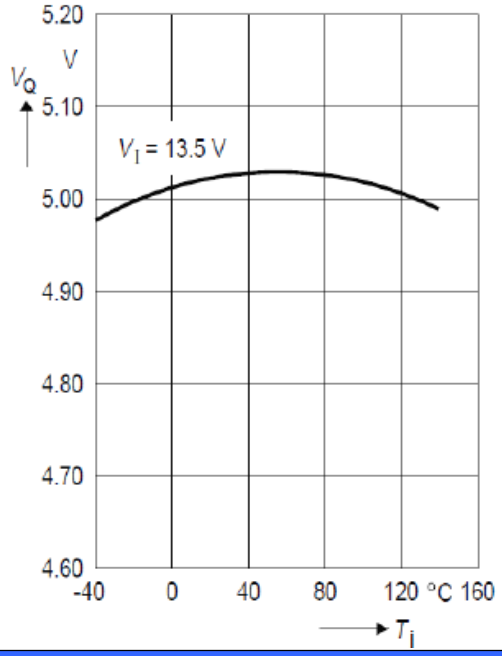
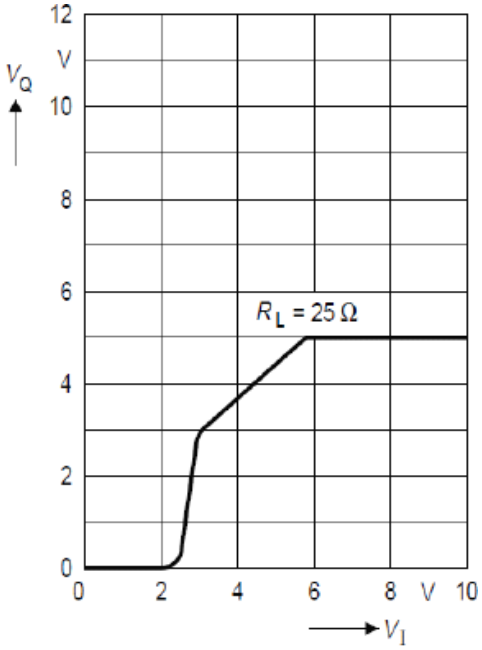
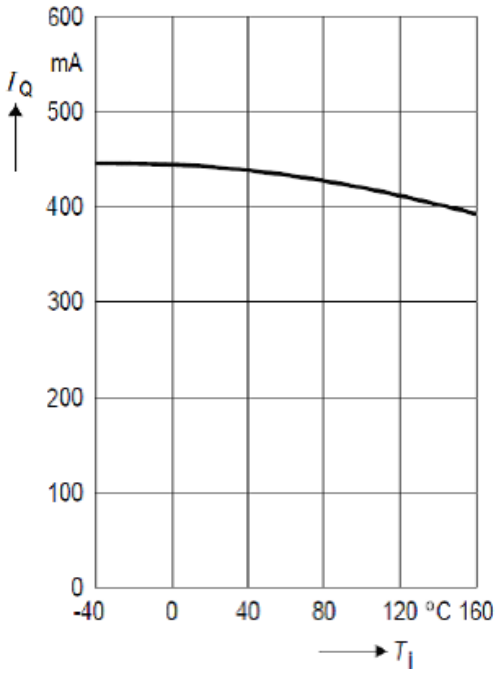
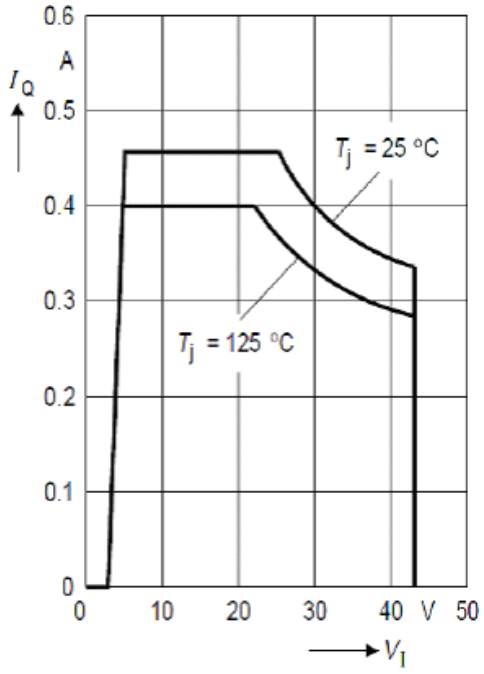
Table 5.1 Electrical characteristics

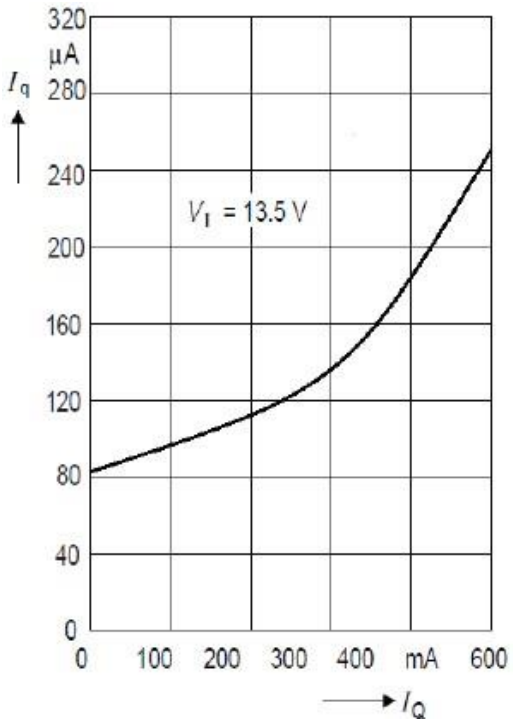
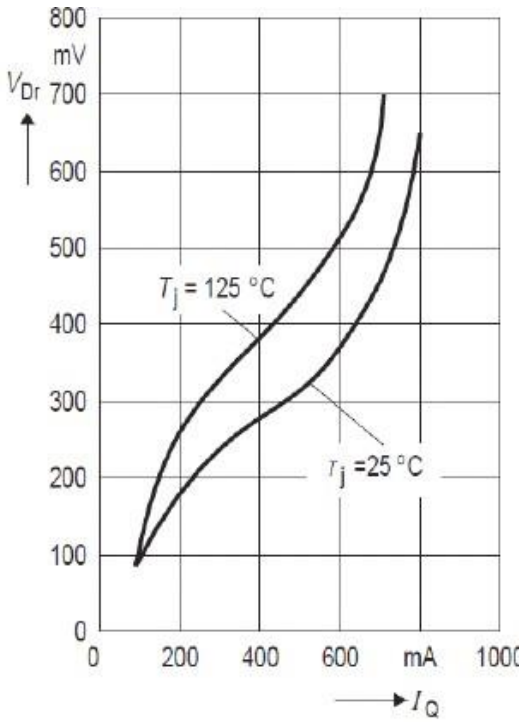
VI = 13.5V，IQ=10mA；-40℃≤Tj≤150℃, unless otherwise specified.

Parameters	Symbols	Limiting value			Unit	Testing conditions
		Min value	Typical value	Max value		
Output voltage	VQ	4.9	5.00	5.1	V	10≤IQ≤400mA； 6.4V≤VI≤16V
			5.0		V	10≤IQ≤400mA； 16V≤VI≤40V
Linear adjustment rate	ΔVQ		5	15	mV	6.4V≤VI≤40V
Load adjustment rate	ΔVQ		9	45	mV	10mA≤IQ≤400mA 1) VINVI=VQnom+Vdr
Voltage difference	Vdr		0.3	0.5	V	IQ = 300mA 2)
Quiescent current	Iq		90	120	uA	IQ=10mA
Output current limiting	IQ,max	400		1100	mA	VI-VQ<18V; VQ=Vnom-100mV
RMS output noise			30		ppm	VQ ppm Tj=25℃ 10Hz≤f≤10KHz
Power supply rejection ratio	PSRR		65		dB	Fr = 120HZ Vr = 0.5Vpp

1) The junction temperature keeps constant during testing.

2) Voltage difference = VI–VQ (it is tested when 100mV drop when compared with the rated voltage at VI = 13.5V).

Output voltage VQ VS junction temperature Tj	Output voltage VQ VS input voltage V1
	
Output current IQ VS junction temperature Tj	**Output current IQ VS input voltage V1**
	

Quiescent Iq VS current output current IQ	Voltage difference Vdr VS output current IQ
	

6. Applications Information

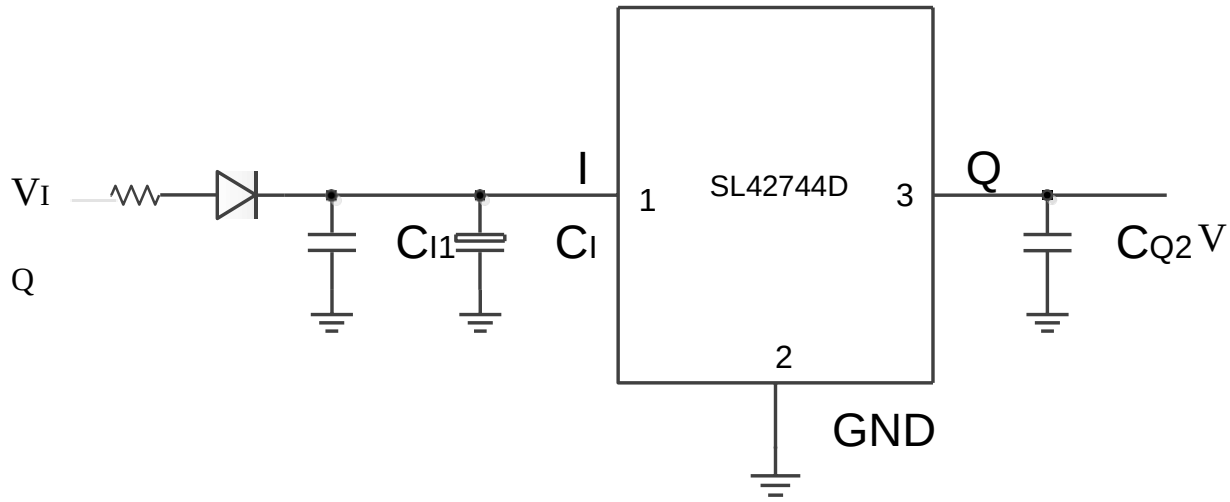


Figure 6-1 Typical application circuit

6.1 Input capacitor

It is suggested to set a ceramic capacitor of 100nF~470nF at the input end, to effectively eliminate the high-frequency interference in the circuit; at the same time, it is suggested to set a electrolytic capacitor of 10~470uF at the input end as the input buffer, so as to smoothen input high energy pulse.

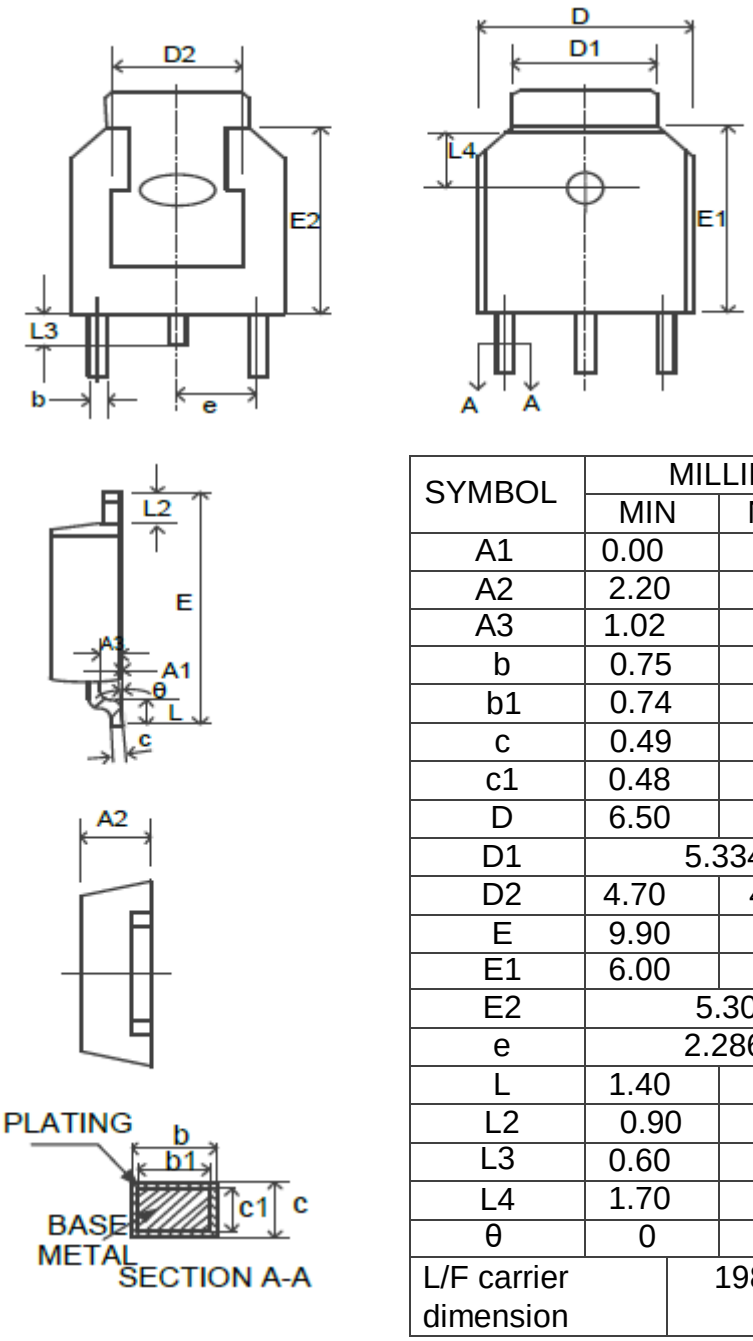
Try to make the input capacitor get close to the pin of the chip.

6.2 Output capacitor

The stability of the output capacitor is essential to the linear voltage regulator, and the electrolytic capacitor or the paster capacitor larger than 10uF can be adopted according to different application conditions.

Try to make the output capacitor get close to the pin of the chip.

7. Package dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A1	0.00	----	0.10
A2	2.20	2.30	2.40
A3	1.02	1.067	1.12
b	0.75	----	0.84
b1	0.74	----	0.79
c	0.49	----	0.57
c1	0.48	0.508	0.52
D	6.50	6.60	6.70
D1	5.334 REF		
D2	4.70	4.826	4.92
E	9.90	10.1	10.3
E1	6.00	6.10	6.20
E2	5.30 REF		
e	2.286 BSC		
L	1.40	1.50	1.60
L2	0.90	----	1.25
L3	0.60	0.80	1.00
L4	1.70	1.80	1.90
θ	0	----	8°
L/F carrier dimension	198*133		

Figure 7-1 Package TO252-3