1.Function Description

The SL4275 is a monolithically integrated low-dropout fixed voltage regulator in a 5-pin TO package. Input voltages up to 55V are regulated to an output voltage VQ of 5.0V. The chip can drive 450mA load and has short circuit protection and over temperature protection. When the output voltage VQ is lower than the typical value of 4.65V, the RQ pin of the chip will generate a low-level reset signal, and the reset delay time can be set by the D pin delay capacitor.

1.1, External component information

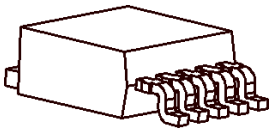
The SL4275 requires an input capacitor CI to compensate for trace effects. In order to ensure the stability of the regulation circuit, the output capacitor C_Q is necessary. Output capacitors with $C_Q \geq 22uF$ and ESR $\leq 5\Omega$ guarantee stability over the operating temperature range.

1.2. Circuit description

The control op amp compares the reference voltage with a voltage proportional to the output voltage and drives the gate of the series MOS transistor through a buffer. In addition, a current-limiting control unit for the load current prevents oversaturation of the power components. The chip also integrates many internal circuits for overload, over-temperature, and other protections.

1.3.Features

- Rated output voltage 5V, accuracy range ±2%
- Ultra-low power consumption: 80uA
- Power-on and Brown-out Reset
- Low drop
- Short circuit protection
- RoHS



TO252-5

2. Principle block diagram

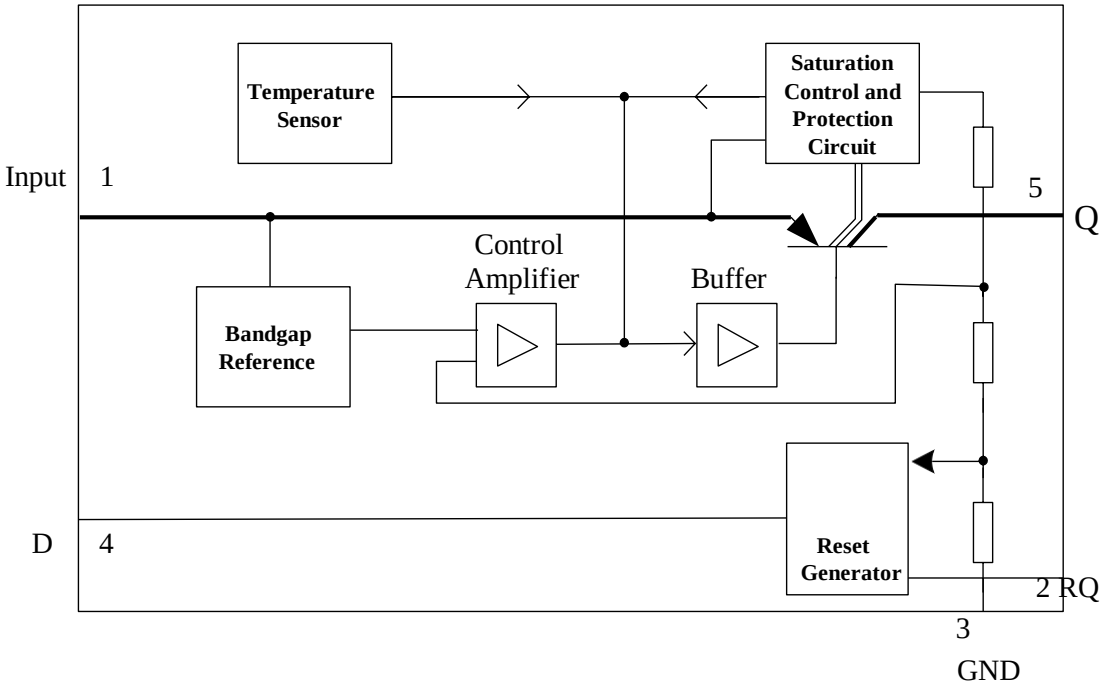


Figure 2-1 Module block diagram

3.Definitions of pins

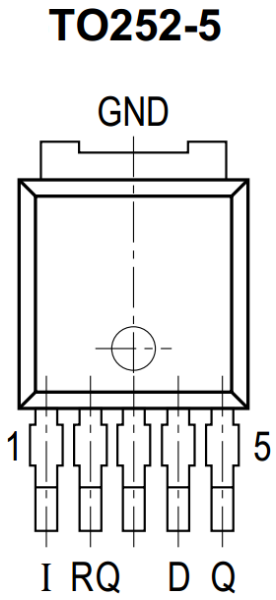


Figure 3-1 Pin configuration (top view)

Table 3.1Pin definition and functions

No. of pin	Symbol	Function
1	I	**Input:** Use a ceramic capacitor to ground directly near the IC side.
2	RQ	**Reset output:** Open-drain output pin requires an external pull-up resistor. When the output voltage is lower than the reset threshold VRT, RQ is pulled low; it can be floated when not in use.
3	GND	**Ground:** Connect to the cooling fin in the device
4	D	**Reset delay** Connect the capacitor to ground to set the reset delay time; it can be left floating when not in use.
5	Q	**Output:** Use a capacitor with CQ≥22uF and ESR<5Ω at 10KHz to connect to ground.

4.General product characteristics

Table 4.1 Absolute Maximum Ratings

Tj=-40℃ to 150℃。 All the voltage values are relative to ground unless otherwise specified.

Parameters	Symbols	Limiting value		Unit	Note
		Min	Max		
Input Voltage	VI	-0.3	60	V	
Output voltage	VQ	-0.3	12	V	
Reset output	RQ	-0.3	36	V	
Reset delay	D	-0.3	12	V	
Temperature	Tj	-40	150	℃	Junction temperature
	Tstg	-40	150	℃	Storage temperature
ESD withstanding voltage	$V_{ESD-HBM}$	-2000	2000	V	Human body mode[1)]
	$V_{ESD-CDM}$	-1000	1000	V	Enabling equipment model [2)]

1) The ESD withstanding voltage human body model is designed according to JESD22-A114.

2) ESD withstanding voltage equipment model is designed according to JESD22-C101E.

Table 4.2 Thermal Resistance

Parameters	Symbols	Limiting value			Unit	Conditions
		Min	Type	Max		
SL 4275 (TO252-5)						
Junction-to-Case Thermal Resistance	RthJC		3.6		K/W	Measurement of the cooling foundation
Junction to ambient thermal resistance	RthJA		27		K/W	
			115		K/W	Only pin
			52		K/W	Cooling fin of 300mm^2
			42		K/W	Cooling fin of 600mm^2

1) It does not refer to production testing, but specially refers to design；

5 Electrical Characteristics

Table5.1 Electrical Characteristics

VI = 13.5V； -40℃ ≤ Tj ≤ 150℃,unless otherwise specified.

Parameters	Symbols	Parameter values			Unit	Testing conditions
		Min	Type	Max		
Working voltage	VI	5.5	13.5	55	V	
Output voltage	VQ	4.9	5.0	5.1	V	IQ<450m;VI<55V
Output current limiting	IQ	450	800		mA	VI=13.5V
Quiescent current	Iq1		80	100	uA	IQ = 5mA
Quiescent current	Iq2		130	160	uA	IQ = 400mA
Voltage difference	Vdr		0.3	0.5	V	IQ = 300mA
Load regulation ratio	ΔVQLo		33	50	mV	5mA<IQ<450mA
Linear adjustment rate	ΔVQLi		2	10	mV	8V<VI<55V,I_Q=5mA
Power supply rejection ratio	PSRR		70		dB	100HZ@0.5Vpp
Output Capacitance	C_Q	1			uF	ESR≤5Ω@10KHZ
Reset output RQ:						
Reset threshold	V_{RT}	4.5	4.65	4.8	V	output voltage drop
Reset hysteresis	Vhys		0.2		V	
Reset response time	t_{rr}			2	us	
Reset output low voltage	V_{RQL}			0.4	V	Rext≥5KΩ ;VQ<VRT
Reset output leakage current	I_{RQ}		0	1	uA	V_{RQ}=5V
Reset delay D:						
Upper trigger threshold	V_{DT}		1.8		V	
Lower trigger threshold	V_{DL}	0.2	0.4	0.6	V	
Delay capacitor charging current	I_{Charge}	3	6	9	uA	V_D=0V
Reset delay time	t_{rd}	10	15	20	ms	C_D=47nF
	t_{rd}		8		us	No capacitors on pins

1) Dropout voltage= VI-VQ (VI-VQ when VQ drops 100mV from the rated output voltage value at VI = 13.5V).

6. Reset function

6.1.Reset threshold（ V_{RT}）

RQ must be connected to an external pull-up resistor. After the chip starts, when the output voltage VQ is lower than VRT, the chip will pull down the reset output pin RQ internally.

When the chip output is shorted to ground, the chip is thermally shut down, or the power supply is under-voltage, this function can feed back a reset low level signal to the MCU.

6.2.Reset response time(t_{rr})

When the output voltage VQ drops below VRT, after trr time, RQ will be set low;

6.3.Reset delay time（t_{rd}）

Before the reset pin (RQ) is set high, connect an external capacitor to the reset delay pin (D). At this time, the D pin will output a constant current (about 6uA) to continuously charge the external capacitor. Until the voltage of pin D exceeds the upper trigger threshold VDT of the internal comparator, at this time RQ will be set high;

If this pin is left floating, the default reset delay time is about 8us.

The reset delay time trd is determined by the external capacitor charging time:

$$t_{rd} = \frac{C_D * 1.8V}{6uA}$$

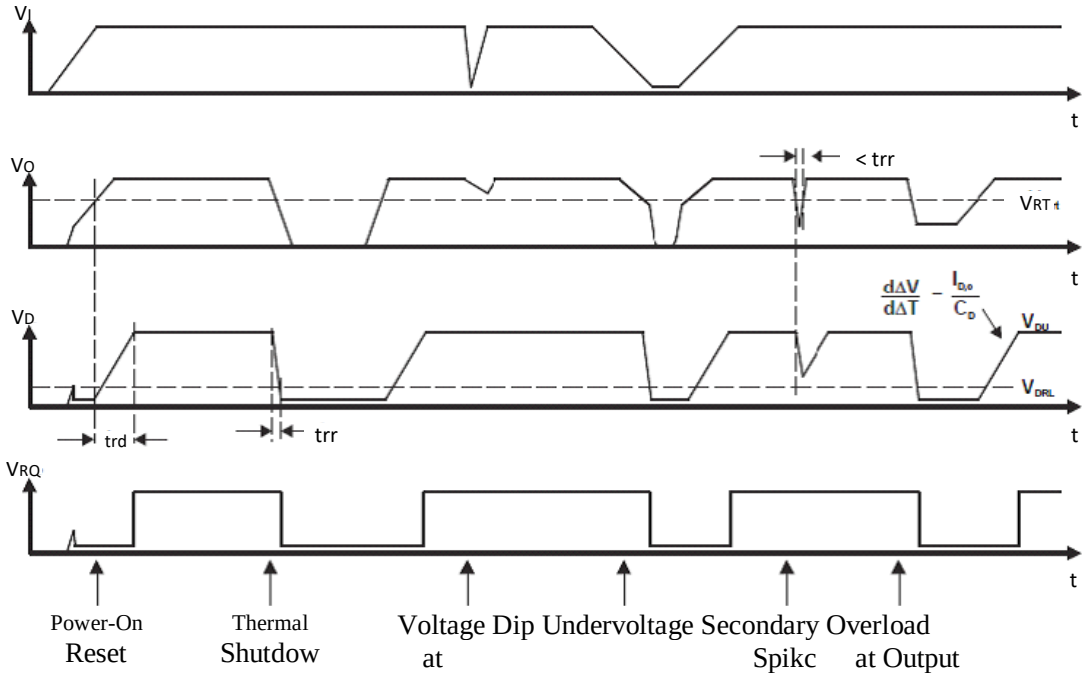
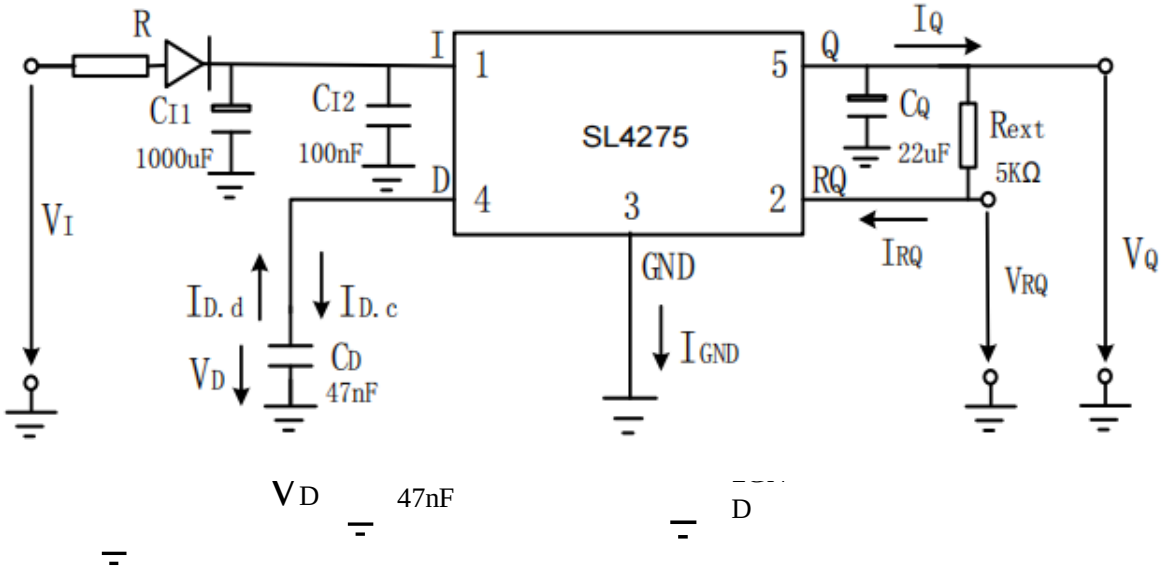


Figure6-1 Reset Timing

7. Applications Information



VD 47nF D

Figure 7-1 application circuit

8.Typical characteristic curve

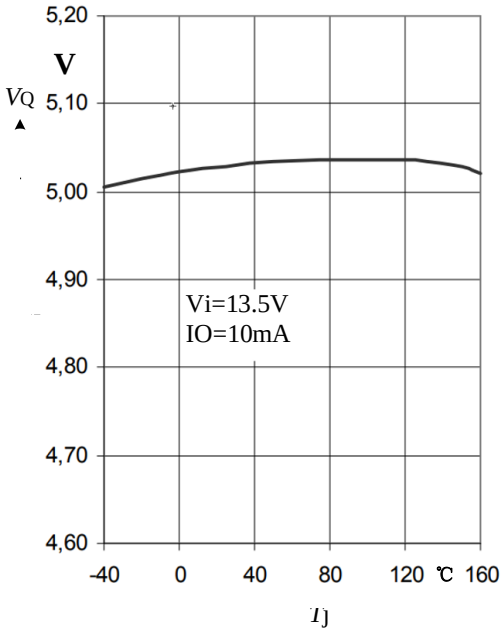


Figure 8-1output voltage VS Junction temperature

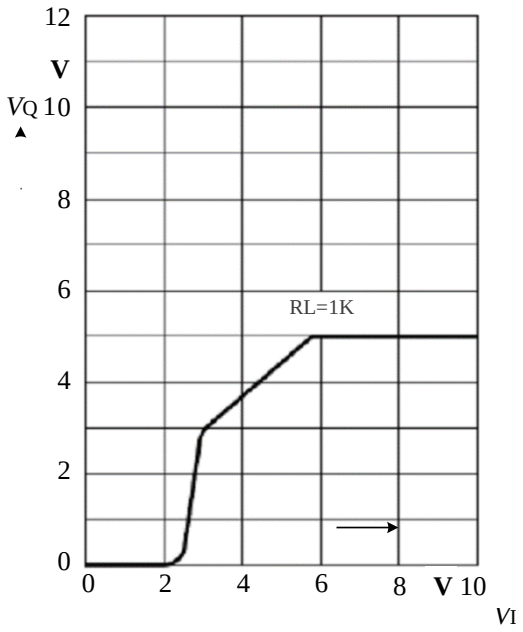


Figure 8-2 Output Voltage VS Input Voltage

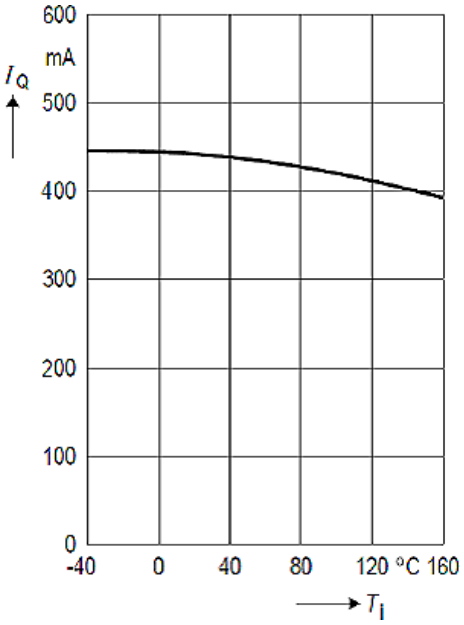


Figure 8-3output voltage VS Junction temperature

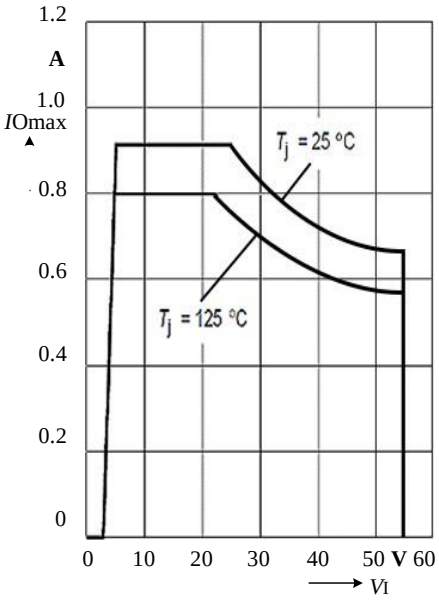


Figure 8-4 Output Current Limit VS Input Voltage

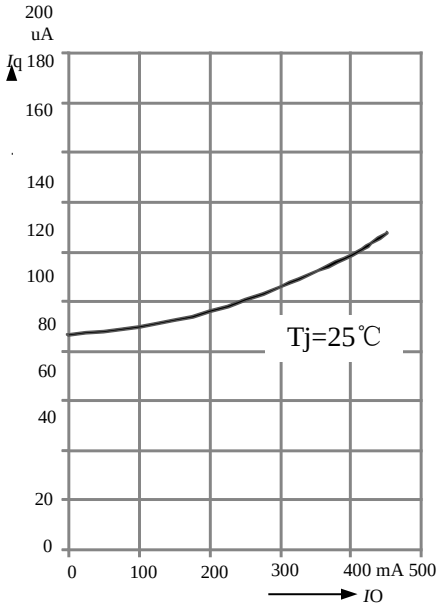


Figure 8-5 Quiescent Current VS Output Current

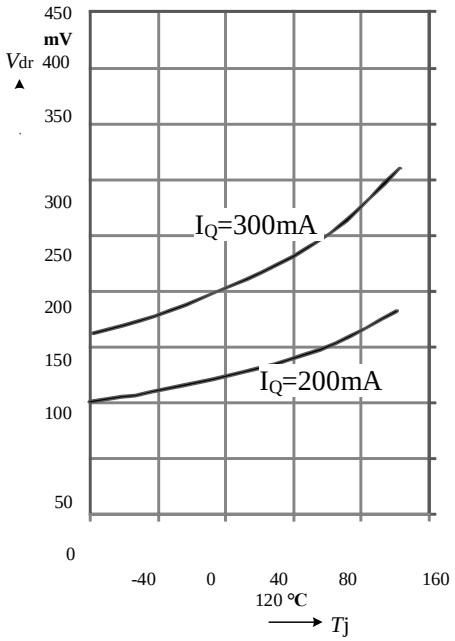


Figure 8-6 Voltage difference VS Junction Temperature

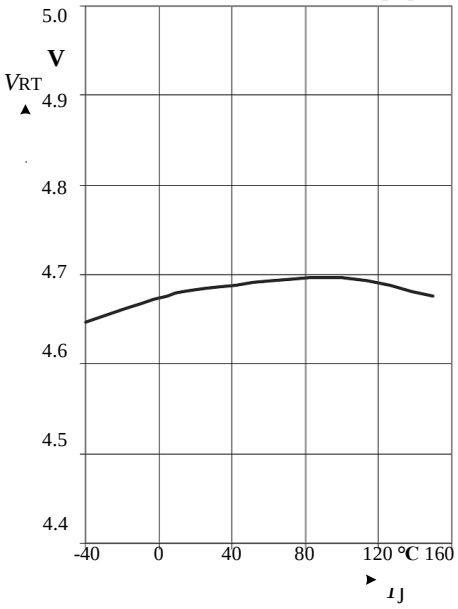


Figure 8-7 Reset Threshold Junction Temperature

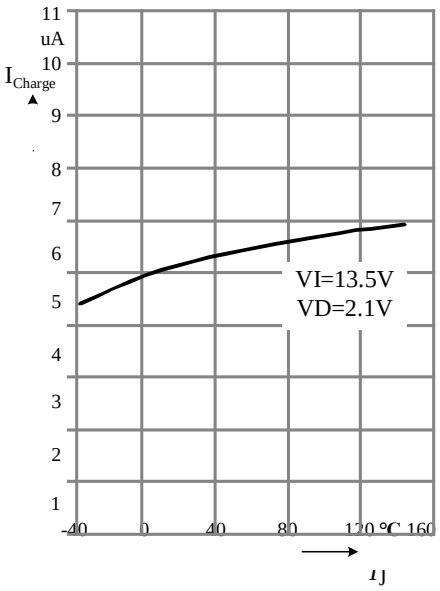
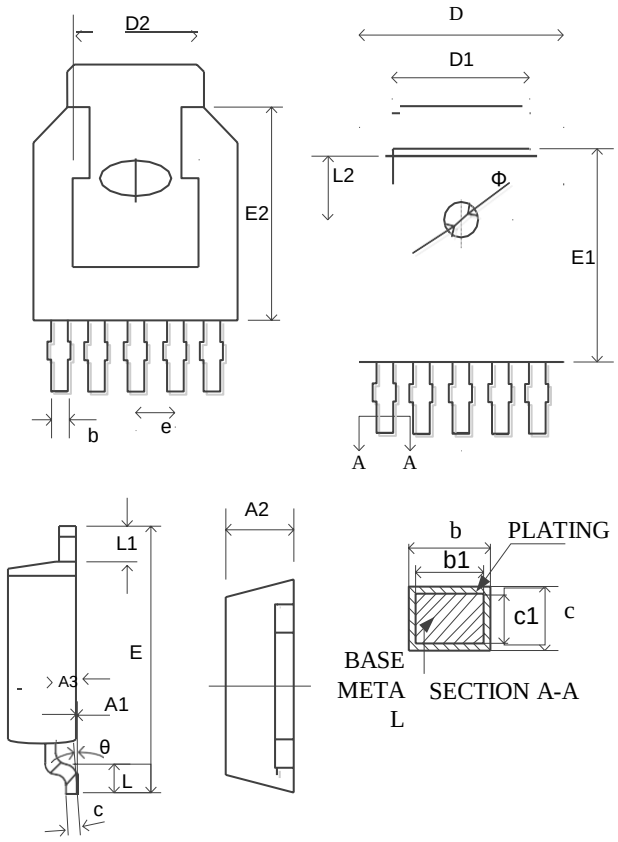


Figure 8-8 Reset Delay Charge Current VS Junction Temperature

9. Package dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A1	0.00	----	0.10
A2	2.20	2.30	2.40
A3	1.02	1.07	1.12
b	0.55	----	0.64
b1	0.54	0.56	0.59
c	0.49	----	0.56
c1	0.48	0.51	0.52
D	6.50	6.60	6.70
D1	5.33 REF		
D2	4.83 REF		
E	9.90	10.1	10.3
E1	6.00	6.10	6.20
E2	5.30 REF		
e	1.27 BSC		
L	1.40	1.50	1.60
L1	1.02 REF		
L2	1.70	1.80	1.90
θ	0	----	8°
Φ	1.20*0.1±0.05DP		

Figure 9-1 TO252-3 Package