25V 4A sourcing current and sinking current Dual

1. Characteristics

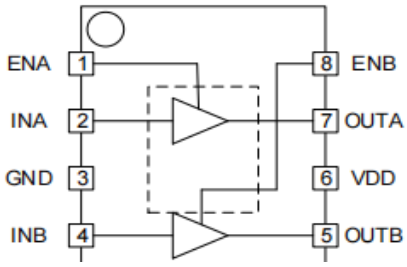
- Dual-channel independent-grid driving
- 4A peak sourcing current and sinking current
- VDD power supply with wide ranges as high as 25V
- Independent enabling input
- Dual channels can be used in parallel for high current drive
- Floating an enable pin enhances parallel accuracy
- VDD under-voltage protection
- TTL and CMOS compatible level inputs
- Low latency (45ns typical) with built-in noise cancellation filter
- 1 ns typical delay match between two channels
- When the input is floating, the output is low
- -40℃ to 125℃ operating temperature range

The SL4427 is a dual 4A high-speed low-side gate driver that efficiently and safely drives MOSFETs as well as IGBTs. Available in SOP-8 packages with or without thermal pads, low propagation delays and mismatches allow MOSFETs to switch in the hundreds of kHz. This chip is very suitable for the synchronous rectification drive of server and communication power supplies, in which the dead time of the synchronous MOSFET directly affects the efficiency of the converter. The driver can increase the output drive current by paralleling two channels. When only one enable pin is enabled high (the other enable pin is floating), the outputs of both channels are driven by a phase-one logic signal. This feature can greatly reduce the mismatch between the two channels and make it suitable for driving parallel switches. The driver's input thresholds are based on TTL levels up to 20V tolerance.

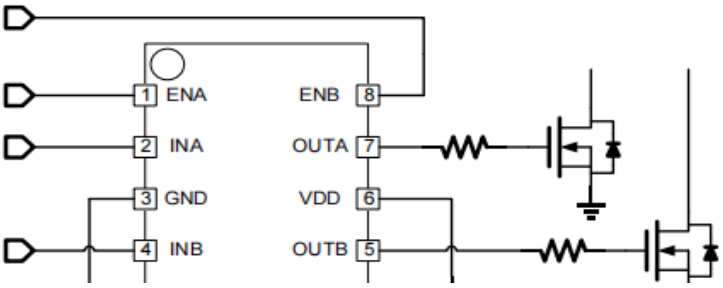
2. Applications

- AC/DC and DC/DC converter
- Server and rectifier for communication equipment
- EV/HEV inverter and DC/DC converter
- PV voltage rise and inverter
- UPS

3. Description



SOP-8 Distribution of pins



Typical applications

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4.Configuration and functions of pins

Pin	Name	I/O	Description
1	ENA	I	A Channel enabling input
2	INA	I	A Channel input
3	GND	G	Ground
4	INB	I	B Channel input
5	OUTB	O	B Channel output
6	VDD	P	Supply voltage
7	OUTA	O	A Channel output
8	ENB	I	B Channel enabling input
	Exposed Pad		Bottom thermal pad is usually connected to GND on the PCB layout Only SOP-8 (EP) packages have

5.Technical indexes

5.1 Absolute Max. rated value

Within the ranges of indoor temperature (unless otherwise specified) (1)

		MIN	MAX	Unit
V_{DD}	Supply voltage (relative to ground)	-0.3	25	V
OUTA, B	Gate drive output voltage	-0.3	V_{DD}+0.3	V
I_{OUTH}	Sink current for gate drive output (10us pulse width and 0.2% duty cycle)		6.6	A
I_{OUTL}	Sink current for gate drive output (10us pulse width and 0.2% duty cycle)		6.6	A
INA, INB,	Signal input voltage	-5.0	20	V
ENA, ENB	Enable input voltage	-0.3	20	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) If the operation exceeds the ranges listed in the "absolute maximum rated value", it may lead to permanent damages to the device. Long-term exposure to the absolute maximum rated value conditions may lead to influences on reliability of the device.

5.2 Anti-static level

			Value	Unit
$V_{(ESD)}$	static electricit discharge	Human body model(HBM)， ANSI/ESDA/JEDEC JS-001 (1)	+/-2000	V
		Charged device model (CDM)， JEDEC specification JESD22-C101 (2)	+/-500	

（1）As specified in JEDEC document JEP155, the standard ESD control process is allowed for safe manufacturing for 500V HBM.

（2）As specified in JEDEC document JEP155, the standard ESD control process is allowed for safe manufacturing for 250V CDM.

5.3 Recommended working conditions

		MIN	MAX	Unit
V_{DD}	Supply voltage	8	20	V
$V_{INx, ENx}$	Signal input voltage	0	18	V
T_A	Environment temperature	-40	125	°C

5.4 Thermal resistance information

	S L4427	Unit
RθJA junction temperature – environment	112	°C/W
RθJA junction temperature –PCB	53	°C/W
RθJB junction temperature – Thermal resistance		°C/W

5.5 Electrical specifications

Unless otherwise specified , V_{DD} = 15 V, T_A = –40°C to 125°C

In the environment of 25°C, in the designated pin, the positive-going current is input, and the inversed current is output.

Parameters	Testing conditions	MIN	Type	MAX	Unit
Bias current					
I_{DDq} Quiescent current	IN=0V		0.75	1.5	mA
Undervoltage protection					
V_{ON} under voltage threshold value	Rise threshold value	6.2	6.7	7.2	V
V_{OFF}	Drop threshold value	5.7	6.2	6.7	
Input (INA, INB)					
V_{INH} input rise threshold value		1.6	1.86	2.1	V
V_{INL} input drop threshold value		1.2	1.48	1.7	V
V_{INHYS} Input hysteresis			0.4		V
V_{INHYS} Negative voltage input		-5			V
enable input(ENA, ENB)					
V_{ENH} Enable Input Rising Threshold		1.6	1.86	2.1	V
V_{ENL} Enable Input Falling Threshold		1.2	1.48	1.7	V
V_{INHYS} Enable Hysteresis Input			0.4		V
Output (OUTA, OUTB)					
I_O (1) Sourcing and sinking current peak	C_{LOAD} =0.22uF, With external current limiting resistor, 1kHz switching frequency		4.0		A
V_{OH} output high level	I_{OUTH} = -100mA	V_{DD}-0.3	V_{DD}-0.13		V
V_{OL} output low level	I_{OUTL} = 100mA	0.2	0.08	0.2	V
R_{OH} pull-up resistance			1.3	3	Ω
R_{OL} output pull-down resistance			0.8	2	Ω
Time series					
TDff drop dela TDff rise dela	Cload = 1.8nF	30 30	45 45	80 80	ns
Tf drop time Tf rise time	Cload = 1.8nF	6 6	13 13	20 20	ns
Tdm (1) mismatch delay	INA=INB, ENA= 5V, ENB floating,		1		ns

(1) Determined by design and characterization, not 100% determined by testing in production.

6 Typical Characteristics

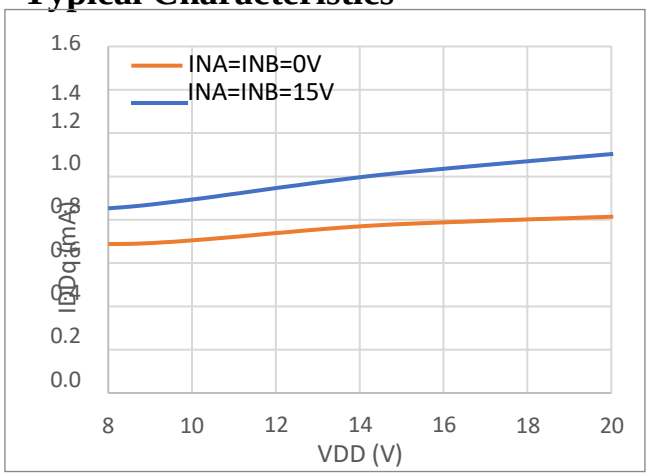


图 1. Quiescent current IDDq vsVDD

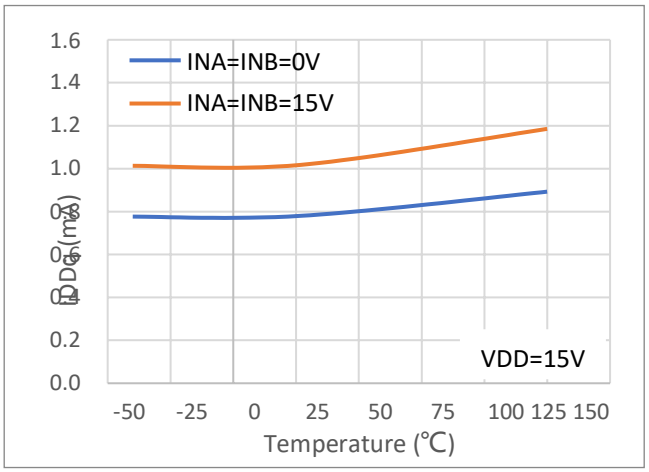


Figure 2. Quiescent current IDDq vs temperature

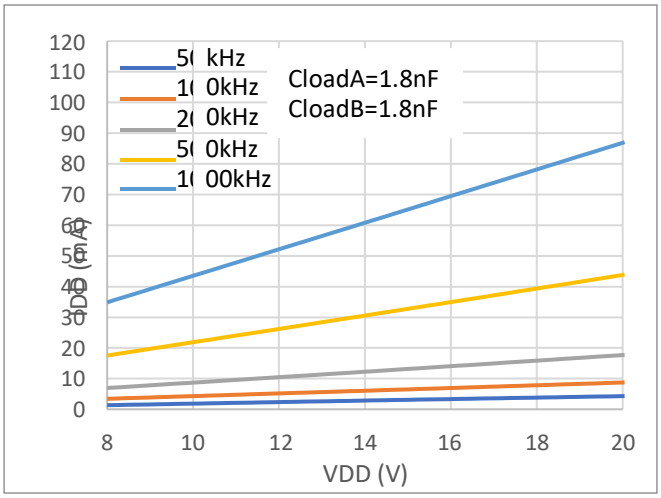


Figure 3. Working current IDD vs VDD

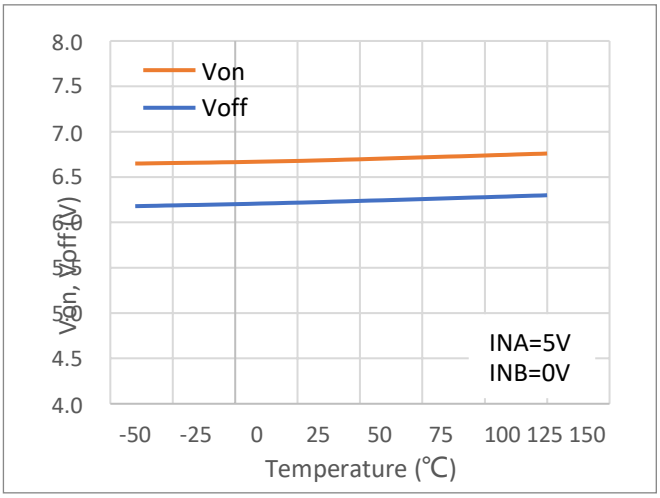


Figure 4. UVLO vs temperature

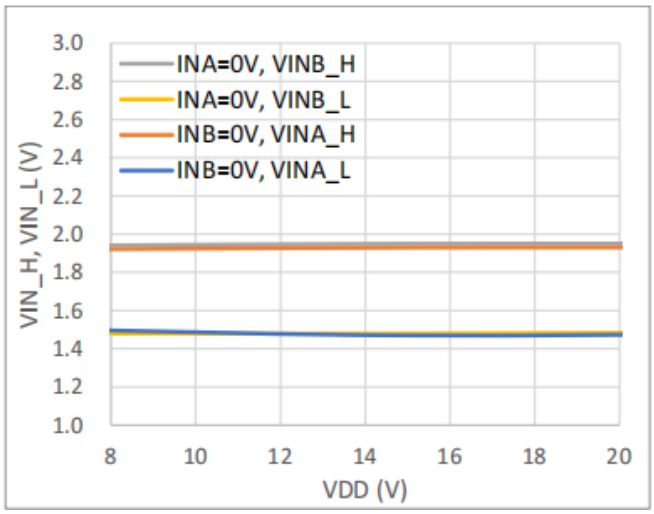


Figure 5. Input Threshold Voltage vs VDD

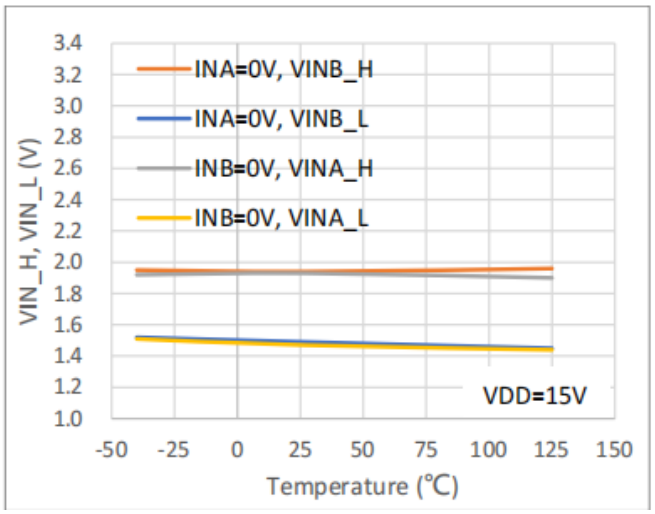


Figure 6. Input Threshold Voltage vs temperature

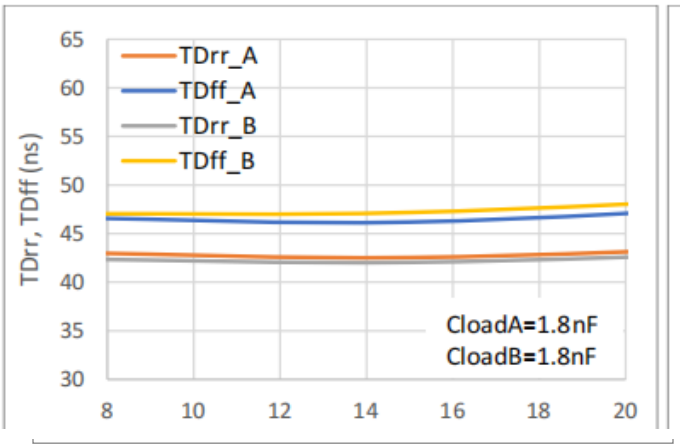


Figure 7. Propagation delay vs VDD

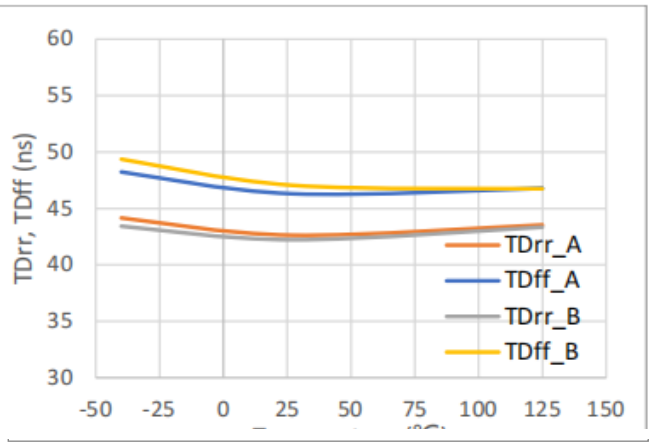


Figure 8. Propagation delay vs temperature

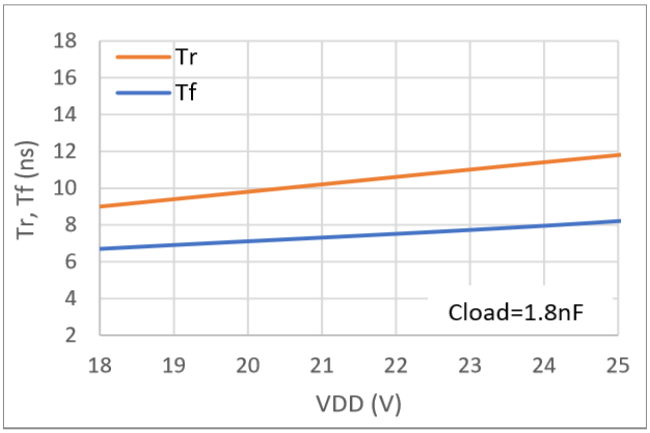


Figure 9. Rise time and drop time vs VDD

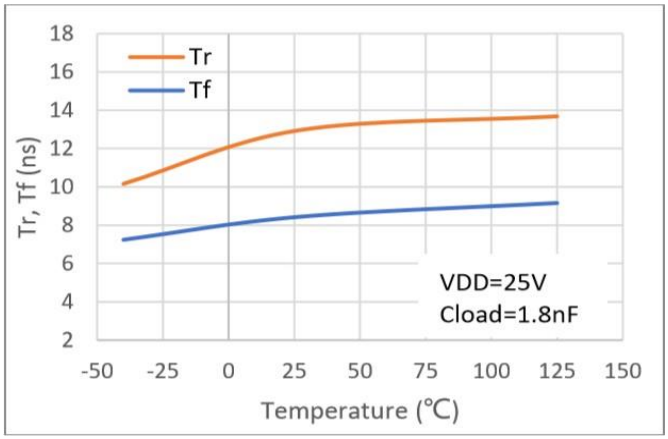


Figure 10. Rise time and drop time vs temperature

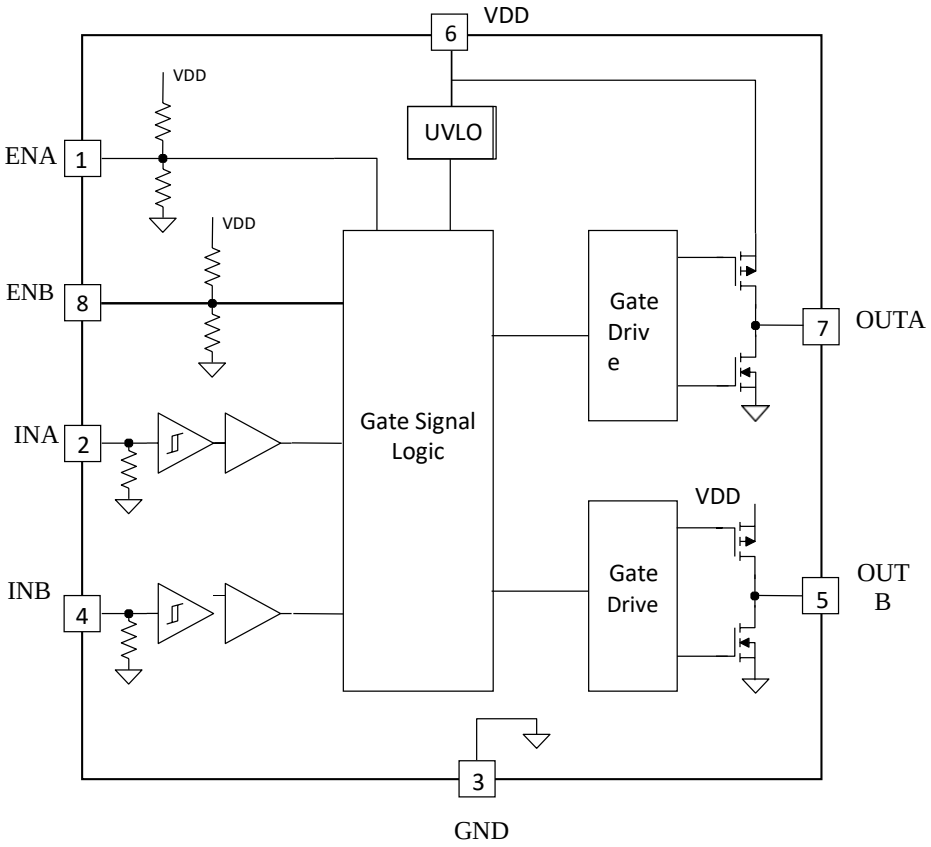
7 Detailed description

The SL4427 drivers provide dual-channel high-speed low-side gate drive. When two channels are connected in parallel to drive high-power or parallel-connected power switches, the three-level enable input can reduce output signal mismatch.

7.1 Signal Input

INA and INB are grid driving input. This pin is a weak pull-down input, if the input is left floating, the output will be pulled to ground. The input is the TTL and CMOS compatible logic level, with the maximum input tolerance of 20V.

Functional block diagram



7.2 ENA and ENB

Compatible to ENA and ENB III level input, When both ENA and ENB are grounded, both corresponding channels are turned off. Both channels are enabled when ENA and ENB are both logic high or floating. When one of ENA and ENB is floating and the other is logic high, their outputs will be driven by the input of the corresponding channel of logic high. This feature ensures low latency mismatch between the two channels.

7.3 OUTA and OUTB

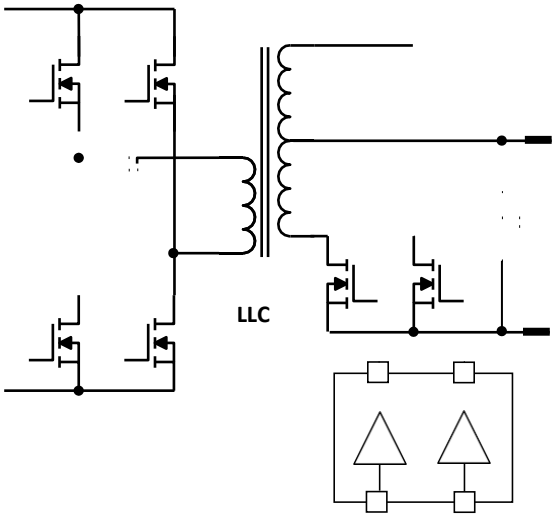
OUTA and OUTB are push-pull outputs, composed by a pair of complexed pull-up P model and N model MOSFET and a pull-down MOSFET. The output of SL4427 can provide the 4A peak value sourcing current and 8A peak value sinking current pulse. The output voltage swings from rail to rail between VDD and GND.

The diode of MOSFET will also provide voltage clamping access to restrain the output voltage to exceed or lower than the ranges. In many conditions, the external Schottky diode clamping is not necessary.

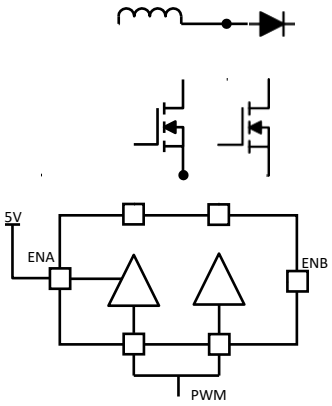
7.4 VDD and undervoltage protection

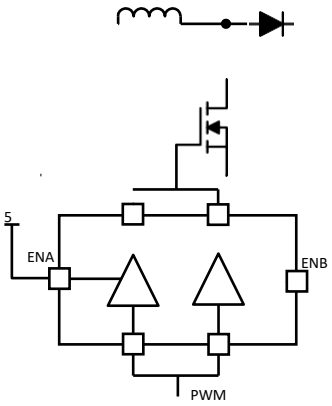
The maximum rated input voltage of the SL4427 is 25V. SL4427 can meet the gate drive of Si MOSFET, IGBT, and SiC MOSFET. The driver has an under-voltage protection function inside. When VDD is below the under-voltage protection threshold, the driver will ignore the input signal and drive the output low.

8 Application and realization



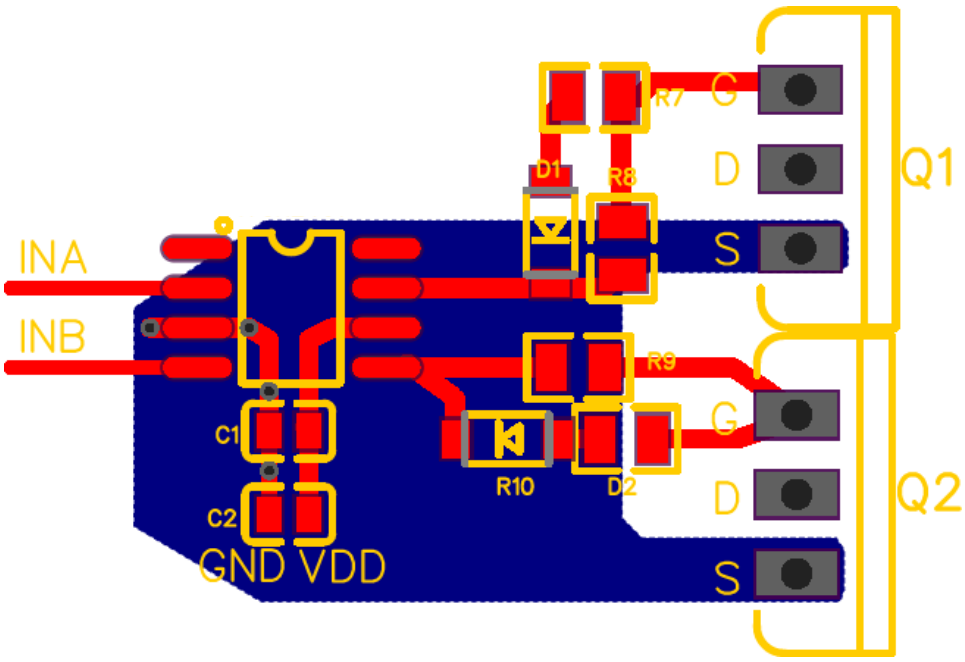
Driving by two channels separately





With minimum mismatch, two outputs drive two switching devices in parallel With minimum mismatch, two outputs drive one high-power switching device in parallel

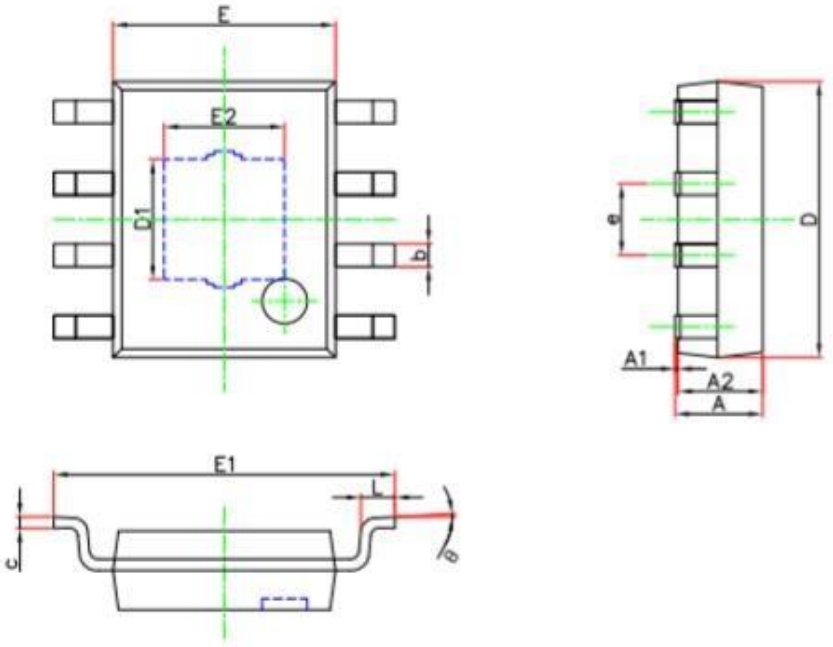
9 PCB arrangement



SL4427Arrangement example

10 Package information

SOP-8 (EP) Package Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.034	2.234	0.080	0.088
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.034	2.234	0.080	0.088
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°